Lecture No 11

Instruction set: Processor Evaluation Matrics

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- **There are four basic issues that determine overall program execution**

1)**Cycle time :** This is primarily a function of implementation technology & secondarily is a function of the instruction set and the size of the unit specified by it.

2)**Cache & memory size bandwidth :** This is primarily a function of the available chip area & the no. of chips involved in the implementation. Secondarily it also is a function of instruction set.

3) **The per instruction execution time:** It is a cycle per instruction. This is primarily determined by the cycle and requirement of instruction set. It is closely related to memory access time, which is determined by cache memory and/or memory configuration.

4) **The no. of instruction required to execute a program**. This is determined by the instruction set & compiler

Program Execution

- Three important constituents of performance are:

1. I- Stream
2. D- Stream
3. The Processor Cycle

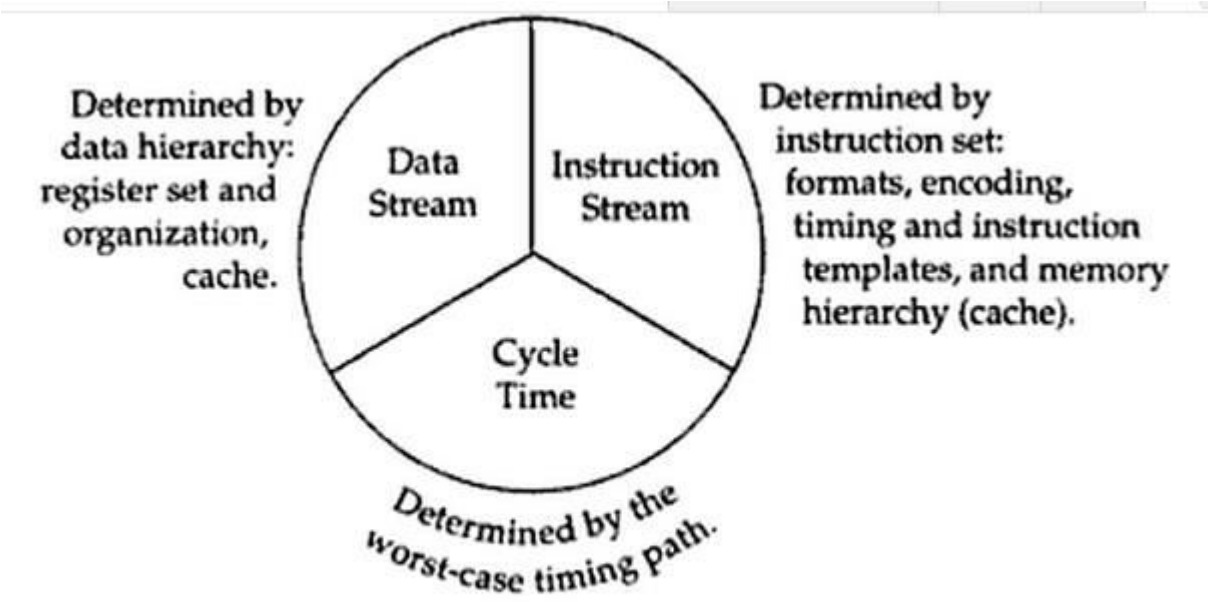

Figure 2.37 Basic performance constituents.

1. Instruction Stream:

- Increasing the no. of formats reduce the no. of instruction executed.
- Increasing the degree of encoding reduced the average size of instruction
- Decreasing the no. of instruction to be executed and average size of instruction decrease the no. of memory access. Require to execute a particular program.

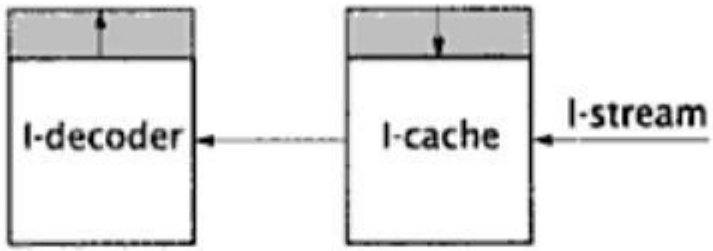

Figure 2.38 I-stream tradeoff: increasing the instruction encoding increases the I-decoder size (area), but decreases the I-cache size (area).

- These factor improves program execution .On the other hand increase the size of instruction decoder & require more sophisticated compiler.
- Multiple instruction sizes and multiple instruction format create difficulty in managing the overlapping & pipelined execution of instruction.

2. Data stream

- A large register set reduces the read & write request to memory, but adding register has a limited usefulness.
- Each additional register is less valuable than a register in initial complement of register.
- In a user requirement with frequent interrupt that result in saving & restoring these register, these additional register can become a burden.
- A large register set size decreases read & write traffic to memory.

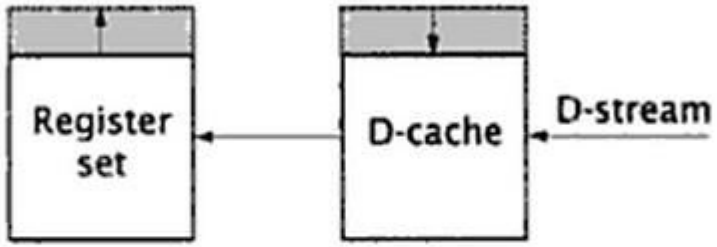

Figure 2.39 D-stream tradeoff: similarly, increasing the register set size decreases the D-cache size.

- However a small register size with a data cache occupying the equivalent amount of areas may provide better overall performance.

3. Cycle time consideration

- Many thing affect cycle time, which is determined by the longest path through the processor logic.
- The longest delay path varies from implementation to implementation, but it usually found in one of the following areas

1) Access time to cache
2) Access to register set
3) Register set access time plus ALU at time.
4) Instruction decode time.